ATTACHMENT B

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/605,605 | 10/13/2003 | Bret R. Dale | BUR920030111US1 | 2604 |

21918 7590 11/18/2005

DOWNS RACHLIN MARTIN PLLC
199 MAIN STREET
P O BOX 190
BURLINGTON, VT 05402-0190

| EXAMINER | |
|---|---|
| ROSSOSHEK, YELENA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 11/18/2005



Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/605,605 | DALE ET AL. | |
| | Examiner | Art Unit | |
| | Helen Rossoshek | 2825 | |

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9,10,12,16,17,19 and 20* is/are rejected.

7)☒ Claim(s) *4-8,14,15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/26/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to the Application 10/605,605 filed 10/13/2003.

2. Claims 1-20 are pending in the Application.

### *Claim Objections*

3. Claims 2, 12 are objected to because of the following informalities: claims 2, 12 recite the limitation "wherein at least some of the plurality of timing paths . . .". There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 2, 11-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to claims 2, 12 Specification fails to support or describe "the step of fixing said early mode problems" before step b), which is inserting a delay element into the timing path, instead paragraph [0023] describes the step of fixing said early mode problems" by inserting a delay element.

As to claims 11, 13 Specification fails to support the limitation ". . . of removing at least one timing path from said portion of the plurality of timing paths".

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 9, 10, 12, 16, 17, 19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Brennan et al. (US Patent 6,434,731).

With respect to claims 1 Brennan et al. teaches a method of reducing the magnitude of an overall instantaneous current draw during a timing cycle in a synchronous integrated circuit having a plurality of timing paths within a method of automated design of a clock distribution network with minimal clock skew (col. 4, ll. 8-11), wherein the clock skew is had a dependency of the voltage level on the path (col. 2, ll.9-19), comprising the steps of: (a) determining for each one of the plurality of timing paths a corresponding delay as shown on the Figs. 4a, 4b plurality of paths (col. 6, ll.35-37), wherein the skew is determined for each path (col. 8, ll.18-20); and (b) inserting a delay element into each one of the plurality of timing paths having said corresponding delay, said delay element configured to induce said corresponding delay into that one of the plurality of timing paths using one of the techniques to reduce clock skew, such as inserting delay into clock distribution network (col. 2, ll.66-67; col. 3, ll.1-7).

With respect to claim 9 Brennan et al. teaches a method of reducing the magnitude of an overall instantaneous current draw during a timing cycle in a synchronous integrated circuit having a plurality of timing paths each having a late mode margin within a method of automated design of a clock distribution network with minimal clock skew (col. 4, ll. 8-11), wherein the clock skew is had a dependency of the voltage level on the path (col. 2, ll.9-19), comprising the steps of: (a) determining if the late mode margin of each one of the plurality of timing paths is greater than zero within determining the skew as a late mode (col. 2, ll.28-30); and (b) for each one of the plurality of timing paths having a late mode margin greater than zero, determining a delay for that one of the plurality of timing paths, said delay being a function of the corresponding late mode margin within determining a specific amount of delay for each timing path considering the difference between the various signal paths (col. 3, ll.2-8).

With respect to claim 16 Brennan et al. teaches an integrated circuit, comprising: (a) a plurality of timing paths each having a late mode margin within determining the skew as a late mode (col. 2, ll.28-30); (b) a delay element located in each one of at least some of said plurality of timing paths, each of said delay elements having a delay that is a function of said late mode margin of the corresponding one of said plurality of timing paths within determining a specific amount of delay for each timing path considering the difference between the various signal paths (col. 3, ll.2-8).

With respect to claims 2, 3, 10, 12, 17, 19, 20 Brennan et al. teaches:

Claims 2, 12: wherein at least some of the plurality of timing paths each have early mode problems (col. 2, ll.37-39), the method further comprising, prior to step (b), the step of fixing said early mode problems (col. 2, ll.60-63; col. 4, ll.3-7);

Claims 3, 10, 17 : wherein each one of the plurality of timing paths has a corresponding late mode margin and step (a) includes setting each said corresponding delay to said corresponding late mode margin (col. 4, ll.18-24);

Claim 19: wherein said plurality of timing paths each have an early mode margin and each said delay is substantially equal to the difference between said late and early mode margins of the corresponding one of said plurality of timing paths (col. 3, ll.4-7; ll.22-24);

Claim 20: wherein at least one delay is substantially equal to the difference between the late and early mode margins of the corresponding one of the plurality of timing paths minus a predetermined period col. 3, ll.4-7; ll.22-24).

***Allowable Subject Matter***

8. Claims 4-8, 14, 15, 18 are allowed. The prior art of record does not teach the overall instantaneous current draw has a profile and step (a) includes setting each one of at least some of said corresponding delays to said corresponding late mode margin minus a fraction of the timing cycle as claimed

***Double Patenting***

9. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis

added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

10. Claims 1-20 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-20 of copending Application No. 10/605,683. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

11. Claims 1-20 are directed to the same invention as that of claims 1-20 of commonly assigned by IBM Application No. 10/605,683. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

Failure to comply with this requirement will result in a holding of abandonment of this application.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

| Title of Invention | HIGH VOLTAGE I/O SIGNAL PROPAGATION BOOST CIRCUIT |
|---|---|

Application Number :
Confirmation Number:
First Named Applicant: Bret Dale
Attorney Docket Number: BUR920030111US1
Art Unit:
Examiner:
Search string: ( 6504418 or 6369613 or 6184716 or 6055414 or 5396128 ).pn

## US Patent Documents

**Note: Applicant is not required to submit a paper copy of cited US Patent Documents**

| init | Cite.No. | Patent No. | Date | Patentee | Kind | Class | Subclass |
|---|---|---|---|---|---|---|---|
| HR | 1 | 6504418 | 2003-01-07 | Coughlin | | | |
| HR | 2 | 6369613 | 2002-04-09 | Costello et al | | | |
| HR | 3 | 6184716 | 2001-02-06 | Depetro et al | | | |
| HR | 4 | 6055414 | 1999-12-21 | Reay | | | |
| HR | 5 | 5396128 | 1995-03-07 | Dunning et al | | | |

## Signature

| Examiner Name | Date |
|---|---|
| Helen Rossoshek | 11/14/2005 |

| Notice of References Cited | Application/Control No. 10/605,605 | Applicant(s)/Patent Under Reexamination DALE ET AL. | |
|---|---|---|---|
| | Examiner Helen Rossoshek | Art Unit 2825 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| * | A | US-6,434,731 | 08-2002 | Brennan et al. | 716/10 |
| * | B | US-2005/0086620 | 04-2005 | Kartschoke et al. | 716/006 |
| * | C | US-6,438,739 | 08-2002 | Yamada, | 716/18 |
| * | D | US-6,446,249 | 09-2002 | Wang et al. | 716/17 |
| * | E | US-6,507,939 | 01-2003 | Andreev et al. | 716/10 |
| * | F | US-6,539,535 | 03-2003 | Butts et al. | 716/17 |
| * | G | US-6,625,788 | 09-2003 | Vashi et al. | 716/6 |
| * | H | US-6,226,774 | 05-2001 | Sawasaki et al. | 716/1 |
| * | I | US-5,764,528 | 06-1998 | Nakamura | 716/6 |
| * | J | US-5,507,029 | 04-1996 | Granato et al. | 716/6 |
| * | K | US-6,651,229 | 11-2003 | Allen et al. | 716/6 |
| * | L | US-6,795,951 | 09-2004 | Hathaway et al. | 716/5 |
| * | M | US-6,510,540 | 01-2003 | Krauter et al. | 716/4 |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
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| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | NN9601397, "Modeling process variation in system-level static timing analysis", January 1996, IBM_TDB, Volume No.: 39, Issue No.: 1, age No.: 397-402 |
| | V | |
| | W | |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

TDB-ACC-NO: NN9601397

DISCLOSURE TITLE: Modeling Process Variation in System-Level Static Timing Analysis

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, January 1996, US

VOLUME NUMBER: 39

ISSUE NUMBER: 1

PAGE NUMBER: 397 - 402

PUBLICATION-DATE: January 1, 1996 (19960101)

CROSS REFERENCE: 0018-8689-39-1-397

**DISCLOSURE TEXT:**

Disclosed is a method for doing **static timing analysis** of electronic systems accounting for the possibility that some chips in the system will, because of manufacturing process variation, operate faster or slower than other chips relative to their nominal speed. This method is a generalization of the method currently used for modelling on-chip process variation during chip-level **static timing analysis**. The modelling of **delay** (process) variation during chip-level **static timing analysis** can be generalized into the following two steps: 1. The **delay** models which represent circuit elements or wires must be able to model the full range of possible **delays** of those elements, from best-case to worst-case. 2. The **timing analysis** program must be able to use the **timing** models in such a way as to select, from the full range of possible **delays**, the appropriate sub-range of **delays** for each element in order to model the desired amount of uncertainty and the correlation between the **delays** of different elements. Statistical methods or "Linear Combination of **Delays**" are two of the ways currently used in **timing** programs to control the selection of the **delay** sub-ranges. When a chip is built, there is a high degree of correlation between the **delays** of the different circuits on the chip. So if the process creates a fast chip, most of the circuits on that chip will have **delays** closer to best-case than the **delays** of circuits on a slow chip. However, the **delays** on a fast chip will not all be exactly best-case. There will be some variation in the **delays**, but they will be correlated close to the best-case end of the spectrum. Similarly, for a slow chip, the circuit **delays** will be correlated near the worst-case end of the range. When doing an **analysis of the timing** behavior of a "slow" chip, it would not be accurate to use worst-case **delays** for all circuits. Consider, for example, a setup test, where the data transition is expected to reach a memory element before the clock transition arrives. It is possible, since the **delays** vary a little bit around worst-case, that when the chip is built, the **delays** on the data path could be slightly slower than usual, while the **delays** on the clock path could be slightly faster than usual. If worst-case **delays** were used in the **analysis** for both the clock path and the data path, the setup test results would be erroneously optimistic. On the other hand, if best-case **delays** were used to model the clock path, and worst-case **delays** were used for the data path, the

setup test results would be unrealistically pessimistic because the delays on a slow real chip will be correlated around worst-case. So, to model the worst possible situation for a setup test on a slow chip, the data path could be modelled with worst-case delays, and the clock path should be modelled with delays a little bit faster than worst-case, somewhere between best-case and worst-case. Similarly, for a slow chip hold test, the clock path could be modelled with worst-case delays and the data path should be modelled with delays between best-case and worst-case. For fast-chip timing analysis, the delays should be correlated around best-case in a similar manner to make both setup and hold times slightly more pessimistic than a pure best-case run. Some static timing analyzers can propagate two sets of voltage transition models through the logic at the same time. One set, called the late-mode transitions, represents the latest possible transitions which could propagate through the logic. The other set, called early-mode transitions, represents the earliest possible transitions which could propagate through the logic. Both of these sets of transitions are propagated through the nets and boxes and are tested against the timing requirements. The basic premise of static timing analysis, as opposed to delay simulation, is "If the latest signal is not too late, none of the signals are too late" and similarly, "If the earliest signal is not too early, then none of the signals are too early." As mentioned above, some timing analysis programs (timers) can propagate and use both sets of transition models in the same run.

If the timer propagates both late-mode and early-mode transition models simultaneously, then the timer can make use of a technique called "Linear Combination of Delays" to account for possible delay variation between elements in the clock and data paths. Using the "Linear Combination of Delays" approach, the late-mode and early-mode sets of voltage transition models are each assigned to use different delays, the timer selecting those delays from the total range of possible delays provided by the element delay models. By using different delays for the late-mode and early-mode transitions, the timer can effectively model the desired uncertainty, or variation, in the delays. For example, to analyze the timing behavior of a "slow" chip, the late-mode transitions could be modelled using worst-case delays, while the early-mode transitions would be "almost worst-case" delays (some user-specified linear combination between best-case and worst-case delays). Similarly, to analyze the behavior of a "fast" chip, the early-mode transitions could be modelled with best-case delays while the late-mode transitions would be a little slower, somewhere between best-case and worst-case. The timing tests are done between the two sets of transitions, to represent the worst possible condition seen in a real chip. So the setup tests are done by comparing late-mode data signals to early-mode clock signals, and the hold tests are done comparing late-mode clock to early-mode data. By using different delays for the late-mode and early-mode transitions, and by comparing the late-mode and early-mode transitions when doing setup and hold tests, the desired amount of variation can be modelled and this variation adds some pessimism to both the setup and hold tests. One implementation of "Linear Combination of Delays" uses a set of six multipliers, A, B, C, D, E, and F, which are specified by the program user. The multipliers are used as follows: where LM = Late Mode EM = Early Mode WC = Worst Case BC = Best Case NOM = Nominal LM_box_delay = A(WC_box_delay) + B(BC_box_delay) + C(NOM_box_delay) EM_box_delay = D(WC_box_delay) + E(BC_box_delay) + F(NOM_box_delay) Typical numbers for a slow-chip analysis may be: LM_box_delay = 1.00(WC_box_delay) + 0.00(BC_box_delay) + 0. 00(NOM_box_delay) EM_box_delay = 0.75(WC_box_delay) + 0.25(BC_box_delay) + 0.00(NOM_box_delay) The multipliers for a fast-chip run would look more like: LM_box_delay = 0.25(WC_box_delay) + 0.75(BC_box_delay) + 0.00(NOM_box_delay) EM_box_delay = 0.00(WC_box_delay) + 1.00(BC_box_delay) + 0.00(NOM_box_delay) Before showing how this method can be applied

to system-level variation modelling, a couple of comments will be made pointing out some important differences between chip-level and system-level timing analysis:

First, at the system level, there could be much less correlation between the delays of individual network elements than at chip level. Second, in a system-level model, several different types of modelling constructs may be used to represent the lower-level circuit elements, whereas in a chip-level model, the lower-level circuits are typically represented only by delay models (timing rules) or by black boxes which are not analyzed. Some of the types of lower-level constructs which may be used in system level models are: delay models (timing rules), black boxes, abstract models, shell abstractions (models which contain only the boundary circuits and boundary timing behavior of the lower-level logic) and full-detail lower-level logic models. The entire system would be represented by a hierarchical logic model (netlist). The individual chips in the system could be represented by any of the lower-level modelling constructs in any desired mixture. The generalized method for modelling process variation in static timing analysis can be applied to system-level models by meeting these two requirements: 1. Regardless of what types of modelling constructs are used to represent the lower-level logic, those constructs must be able to model the full range of possible delays (best-case to worst-case) of the lower-level logic. This range of behavior would be specified differently for the different types of modelling constructs used to represent the lower-level logic. For example, if a chip is represented by a delay rule, the rule must model both the worst-case and best-case timing behavior of the chip. - If a chip is represented at system level by a black box, the full range of chip timing behavior must be specified by worst-case and best-case timing assertions on the black box input and output pins. Similarly, if a chip is represented by a shell abstraction, that shell must include worst-case and best-case timing behavior so that the full range of possible chip timing behavior is represented. If an abstract model is used to represent a chip, that abstract model must contain the necessary information to model the chip in both best-case and worst-case forms. If full chip models are used to represent a chip, two models are required (worst-case and best-case) for each chip in the system which is being so modelled. 2. The timer program must be able to select, from the full range of possible delays, the appropriate delay, with the desired amount of uncertainty, for each lower-level logic element.

The specific examples below show how this method can be applied using "Linear Combination of Delays" and several different types of lower-level modelling constructs: o Delay models (timing rules): Process variation using timing rules at system level would be done exactly as Is described above for chip-level timing analysis, except that the "Linear Combination of Delays" multipliers would be adjusted, as appropriate, to model the desired delay variation for each lower-level element and the correlation between the element delays.

o Black-boxes: The late-mode and early-mode assertions around the edges of the black box would represent the full range of possible timing behavior (worst-case and best-case). These assertions could come from the results of two chip-level timing runs, one using worst-case delays and one using best-case delays. The timer, at the system-level would apply the system level "Linear Combination of Delays" multipliers to the black box boundary assertions before using those values and propagating them into the higher-level logic. This would be done as follows: where the multipliers are A, B, C, D, E, and F AT = Arrival-Time RAT = Required-Arrival-Time LM = Late Mode EM = Early Mode BC = Best Case WC = Worst Case on the left side (input side) of the black box:

sys-level LM RAT = A(LM WC chip RAT) + B(LM BC chip RAT) + C((LM WC chip RAT + LM BC chip RA) / 2) sys-level EM RAT = D(EM WC chip RAT) + E(EM BC chip RAT) + F((EM WC chip RAT + EM BC chip) / 2) and on the right side (output side) of the black box:

sys-level LM AT = A(LM WC chip AT) + B(LM BC chip AT) + C((LM WC chip AT + LM BC chip AT sys-level EM AT = D(EM WC chip AT) + E(EM BC chip AT) + F((EM WC chip AT + EM BC chip AT After system-level timing has been completed, the new late-mode and early-mode arrival and required-times on the black box boundaries would be fed back to the slow-chip and fast-chip chip-level timing runs.

o Shell abstractions: Late-mode and early-mode assertions in the shell model could be used to represent the full range of possible chip timing behavior (best-case to worst-case). The assertions could be generated using two separate chip-level timing runs, a worst-case run and a best-case run. The timer, at the system-level would apply the system level "Linear Combination of Delays" multipliers to the shell model assertions before using those values and propagating them into the higher-level logic. Equations like those shown above for black boxes would be used. After system-level timing has been completed, the new late-mode and early-mode arrival and required-times on the shell boundaries would be fed back as assertions to the slow-chip and fast-chip chip-level timing runs.

o Abstract models: The abstract models would contain the necessary information to model the total possible variation of chip timing behavior. System-level process variation would be modelled by using system-level "Linear Combination of Delays" multipliers with the abstract models, just as is done with timing rules in chip-level timing, described above.

o Full lower-level logic models: Using full detail chip models to model system-level process variation would require two models or two analysis modes for each chip, one worst-case and one best-case, to fully describe the possible variation of the chip's timing behavior. The two chip models would each require its own set of chip-level "Linear Combination of Delays" multipliers which would be different from the system-level multipliers. During the system-level timing analysis, signals would be propagated between the higher-level model and both chip-level models for each chip in the system.

The system-level "Linear Combination of Delays" multipliers would be used at the chip boundaries to convert between the full range of values coming from the two lower-level chip models, and the values which apply to the specific system-level conditions in effect for the run.

This conversion would be done as follows: on the left boundary of each chip: sys-lvl LM RAT = A(WC chip LM RAT) + B(BC chip LM RAT) + C((WC chip LM RAT + BC chip LM RAT2) sys-lvl EM RAT = D(WC chip EM RAT) + E(BC chip EM RAT) + F((WC chip EM RAT + BC chip EM RAT2) and on the right boundary each chip:

sys-lvl LM AT = A(WC chip LM AT) + B(BC chip LM AT) + C((WC chip LM AT + BC chip LM AT ) / sys-lvl EM AT = D(WC chip EM AT) + E(BC chip EM AT) + F((WC chip EM AT + BC chip EM AT ) /

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